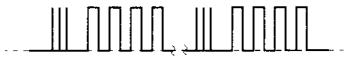
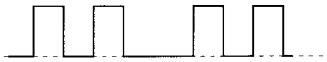
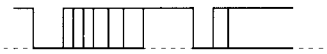
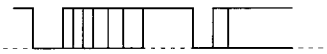
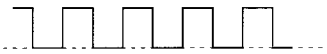
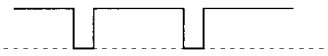
TP	Name	Signal	Freq/Per	Description
171	MS1		varying	Address line for standard RAM and ROM; pulse trains at 20 ms, low pulses 0.6 µs
172	MS2		varying	Address line for standard ROM; pulse trains at 200 ms
173	MS3	0V	DC	Address line for standard ROM D1220; shows pulses if D1220 (FROM type 28F200 or 28F400) is installed
174	SCEN		varying	Chip enable signal for external RAM; pulse width 0.4 µs
175	FCEN		varying	Chip enable signal for standard ROM; pulse width 0.1 µs
176	BCEN	-	-	not used
177	XCEN		varying	Chip enable signal for standard RAM; min. pulse width 30 ns
180	A00		varying	Address lines A00
.	.			up to
.	.			
.	.			
194	A14			A14
201	µPCLK		12.5 MHz	Microprocessor clock
202	MASKN	+5V	DC	Mask not input. If made low, only µP-ROM program runs (FlashROM software does not run)
203	WEN		varying	Write signal for D-ASIC and EXTERNAL RAM Pulses 100 ... 200 ns
204	REN		12.5 MHz	Read signal for D-ASIC and EXTERNAL RAM
208	+5VUP	+5V	DC	µP supply
210	RESETN	+5V	DC	Reset line, is kept low after power on until +5V supply is at 4.7V